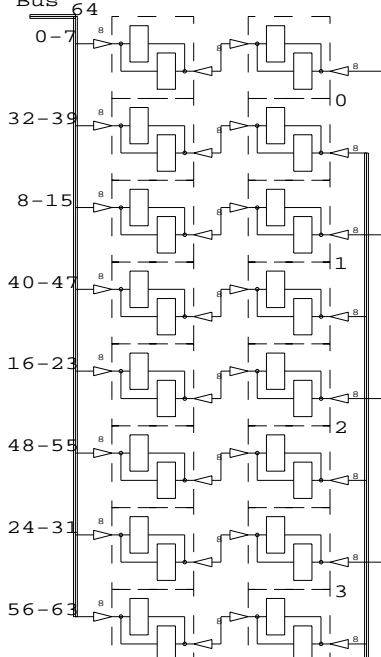


DOUBLE BUFFER FORMATTER

BUF 1 BUF 2
Memory B <-> A B <-> A
Bus 64

(SELECT BY BYTE,
NIBBLE, MORSEL,
OR BIT, AND TAG.)



DATA/TAG
MASK IN
FORMAT
REGISTER

R.FMT[0..1]

NOTE: ROTATE RIGHT 1
FROM FORMATTER
TO INTERPOLATOR

Byte Nibble Morsel/
Mux Mux Bit Mux

FORMATTER SEQUENCER

M.BUF1A.WT- M.BUF2A.WT-
MM.DCK.P M.BUF2B.WT-
R.BUF1.SELAB R.BUF2.SELAB
R.BUF1.SELBA R.BUF2.SELBA
M.BUFDIR

M.FMT.CTRL0
M.FMT.CTRL1
M.INT.CTRL0
M.INT.CTRL1

M.WRD.SEL0
M.WRD.SEL1

3 2 1 0 HB LB

WTSEL

3 2 1 0

RDSEL

3 2 1 0

LOCAL DATA LD[0..15]

MAIN
DATA
BUS

INTERPOLATOR

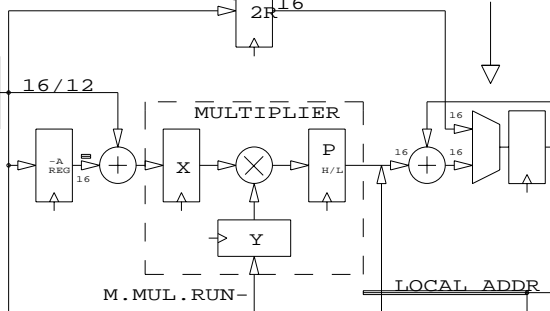
(COMPUTES A+X(B-A))

VARIABLE TAG DELAY

8 IT[0..7]

2R 16

INTERPOLATOR
ACCUMULATOR



M.MUL.RUN-

LOCAL ADDR

IT[4..7]

ACV[3..6]

IT[0..3]

BW BITS

IN.VOL
M.LUTC.S1
R.LUTC.S2
SLICE

INTACC

LOGICAL
SHIFT LEFT
TO BUS

ADDER MULTP

DT LUTS

(SELECTED BY LA[14..15])

LOCAL ADDRESS LA[0..19]

12

LUT
A
00

LUT
B
01

DT.DATA
8

M.VALID
DATA.VALID
TAG.VALID

DT.TAG
8

DT.LABEL
4

2R 4

DTLUT

DTLUT

DTLUT

DTLUT

DTLUT

Dynamic Digital Displays 130 Radnor-Chester Rd. St. Davids, Pennsylvania 19087			
Title	DT Block Diagram		
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Date:	March 6, 1992	Sheet	of

