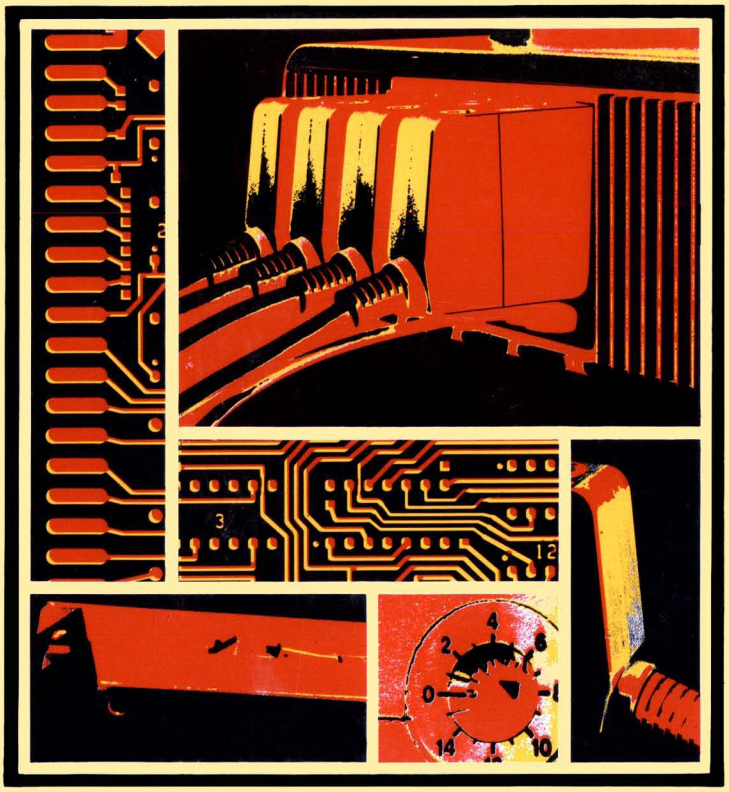
Series 9800 Desktop Computers

HP 98034
Installation and Service



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98034 HP-IB Interface
Installation and Service Manual

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Chapter 1

General Information

Introduction

The HP98034 HP-IB Interface connects an HP desktop computer (9825, 9835 or 9845) to the HP Interface Bus. The interface conforms to the IEEE Standard 488-1978[1], allowing the desktop computer to perform a wide variety of operations via an HP-IB system. The terms computer, desktop computer and calculator are used interchangeably in this manual, and refer to an appropriate HP 9800-series computer.

This manual describes how to install and service the 98034 interface. In addition, a general description of HP-IB operations is given in the following pages. This manual replaces the 98034A Interface Manual, 98034-90000. All previous versions of the 98034A Interface are covered here.

98034A (Plastic Case)

The 98034A Interface was revised (rev. E and later) to improve the interface reliability and interrupt service. This revised version of the 98034A is compatible with 9835 and 9845 Desktop Computers. Replacement parts, component locators, and logic diagrams are shown for both versions of the 98034A.

> **NOTE**
> The unrevised version of the 98034A (rev. D and prior) will not function properly with 9835 and 9845 Desktop Computers.

98034B (Metal Case)

The 98034B Interface is functionally identical to the 98034A. The metal-case 98034B Interface provides reduced electromagnetic radiation interference (EMI). Logic diagrams and component locators are identical to the 98034A rev. E interface. A replacement parts table for the 98034B is provided.

[1] IEEE Standard Digital Interface for Programmable Instrumentation. This standard describes the functional, electrical, and mechanical elements of the HP-IB system.

Field upgrade kits are available for desktop computers to provide the necessary ground connections for the 98034B Interface. The upgrade kit need only be installed when reduced EMI is required. Contact your local HP Sales and Service office for details.

Low EMI Upgrade Kits

Computer	Upgrade Kit
9825	98273A
9835	98373A
9845	98473A

I/O ROM Cards

The I/O ROMs plugged into the calculator determine which bus operations can be performed. For example, the General I/O ROM for the HP 9825A Calculator provides control of one instrument at a time on the bus. Use of the Extended I/O ROM, however, enables complete control of bus functions. After the interface is connected as described in Chapter 2, refer to the appropriate I/O ROM manual for all bus-control operating instructions.

Technical Specifications

The bus card's electrical characteristics are listed below. For complete details on HP-IB electrical, mechanical, and timing requirements, refer to IEEE Standard 488-1978.

Select Code

The bus card is preset to select code 7 at the factory. A switch permits changing the setting, if necessary.

Addresses

The bus card is preset to ASCII talk address "U" and listen address "5". Any one of 30 other pairs of talk/listen addresses can be switch-selected on the card.

Bus Signal Lines

The bus consists of 16 signal lines as follows:

The pin-outs on a standard HP-IB cable are shown below.

Table 1. HP-IB Signal Lines

DIO1	Data Input/Output 1
•	•
•	•
•	•
DIO8	Data Input/Output 8
DAV	Data Valid
NRFD	Not Ready for Data
NDAC	Data Not Accepted
IFC	Interface Clear
ATN	Attention
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify

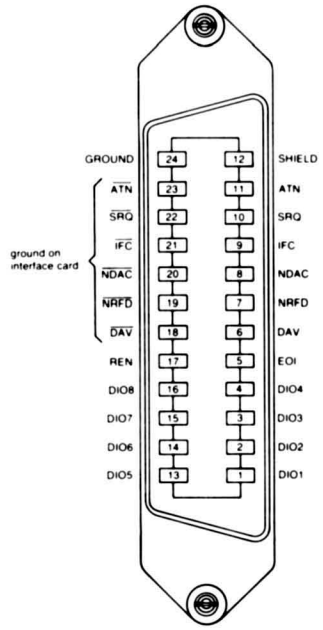


Figure 1. HP-IB Cable Pinouts

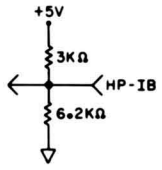
Logic Levels

All signals use negative-true logic (low = logical 1) ◗

High >2.4V
Low <0.4V

Line Termination

Each of the 16 bus signal lines is terminated as shown here ◗



Line Drivers

Each of the signal lines has a driver circuit with the following characteristics:

Type:	Open Collector
Output Voltage Low State:	<0.4 V @ 48 mA
Output Voltage High State:	>2.4 V @ −5.2 mA

Line Receivers

Each of the signal lines is received with a circuit having the following characteristics:

Hysteresis:	V_t pos. − V_t neg. ≤0.4 V
Low State:	Negative Threshold voltage V_t neg. ≥0.6 V
High State:	Positive Threshold voltage 2.0 V ≥V_t pos.

Cable Length

A 4-meter cable is supplied with the card. Also see "Cable Length Restrictions" in Chapter 2.

Operating Temperature

0 − 55° C

Power Requirements

The calculator supplies all power for the card.

Bus Functions and Messages

The following table lists the HP-IB functions and the capability available with the bus interface. A complete description of these interface functions can be found in the IEEE Standard 488-1978.

Table 2. Bus Functions Available with the 98034

Function	Implementation
SH1 (Source Handshake)	Complete Capability.
AH1 (Acceptor Handshake)	Complete Capability.
T6 (Talker)	Basic Talker. Serial Poll. Unaddress if my listen address (MLA).
L4 (Listener)	Basic Listener. Unaddress if my talk address (MTA).
SR1 (Service Request)	Complete Capability.
RLØ (Remote-Local)	Not Implemented.
PP2 (Parallel Poll)	Omits capability of being configured by controller.
DC1 (Device Clear)	Complete Capability.
DTØ (Device Trigger)	Not Implemented.
C1,2,3,4,5 (Controller)	System Controller. Send Interface Clear (IFC). Send Remote Enable (REN). Respond to Service Request (SRQ). Send Interface Message. Receive Control. Pass Control. Parallel Poll. Take Control Synchronously.

The interface and calculator I/O ROMs determine how these functions are implemented to generate messages for controlling the bus. Some functions are not available to the user with certain calculator I/O ROMs. In many cases, the I/O ROM and interface handle the functions automatically, as required, to simplify bus operation for the user.

Here is a complete list of bus messages and their corresponding bus command or line name as described in previous HP-IB manuals. Refer to the appropriate I/O ROM manual for more details.

Table 3. HP-IB Messages

Message (command or line)	Description
Data	Transfer instrument-dependent information between a talker and one or more listeners. It may be instrument programming information or data readings.
Trigger (GET)	Signals a group of selected devices to simultaneously initiate a set of device-dependent actions.
Clear (DCL or SDL)	Causes an instrument to be initialized to a predefined or power-up state (a certain range, function, etc.)
Remote (REN)	Enables remote operation of all devices, allowing parameters and device characteristics to be programmed via data messages.
Local (GTL)	Causes selected instruments to switch to local (front or rear panel) control.
Local Lockout (LLO)	Prevents local (front or rear panel) control of instrument functions.
Clear Lockout/Local ($\overline{\text{REN}}$)	Removes all devices from Local Lockout mode and causes all devices to revert to manual control. See the following note.
Require Service (SRQ)	Indicates a device's need for interaction with the controller.
Status Byte	Transfers a byte (8 bits) of status information to a listener. One bit indicates whether or not the device is currently sending the require service message. The other 7 bits (optional) indicate device-dependent status.

(Continued)

Table 3. HP-IB Message (cont.)

Message (command or line)	Description
Status Bit	Transfers a single bit of device-dependent status, which may be logically combined with other Status Bit messages to the controller.
Pass Control (TCT)	Passes bus controller responsibilities from the current controller to a device which can assume the bus supervisory role.
Abort (IFC)	Halts all bus operation and causes control to unconditionally pass back to the system controller.

NOTE

When the 9825 Calculator is the system controller, pressing [RESET] automatically outputs the Abort and Clear Lockout/Local messages.

Data Transfer Rate

The 98034 Interface transfers data at the rate of about 45 Kbytes (8-bit characters) per second. The actual I/O rate can be considerably slower, however, and is determined by the talker and listener(s) on line at any given time. The slowest device always determines the actual data rate.

Chapter 2
Installation

Unpacking and Inspection

If the shipping carton is damaged, ask that the carrier's agent be present when the interface is unpacked. Inspect the interface for damage. If the interface is damaged or fails to meet electrical specifications, immediately notify the carrier and the nearest HP sales and service office (offices are listed at the back of this manual). Retain the shipping carton and padding material for the carrier's inspection. The sales and service office will arrange for the repair or replacement of your interface without waiting for the claim against the carrier to be settled.

Installation

Before plugging in the bus card, verify that its address and function switches are set to your system's needs. The switches are preset at the factory as follows:

Table 4. 98034 Factory Settings

Switch	Function	Factory Setting
A1S1	Select Code	7
A1S2	Parallel Poll Sense	Neg-True Logic (position 1)
A1S3 (1–5)	Calculator Address	Talk = U, Listen = 5 (off, on, off, on, off)
A1S3 (6)	System Controller	Enabled (on)
A2S1	Parallel Poll Bit	Bit 1

Changing any of the switch settings except select code requires opening the interface case; see page 10 for instructions.

After verifying (or changing) the switch settings, install the card as follows:

1. Switch the calculator off.
2. Insert the bus card into any one of the I/O slots at the back of the calculator. Press the card firmly into the slot.
3. Verify that the required I/O ROM is plugged in to provide the calculator with bus control; see the manual furnished with the ROM.
4. Switch the calculator back on.

Interconnecting Cables

A 4-meter cable is supplied with the bus card. The piggy-back connector end is connected to the peripheral device. Other devices may be added to the bus by using either the standard or the new low-EMI bus cables listed below.

Length	Accessory Number	
	Standard	Low EMI
10.5 meter	–	10833A
1 meter	10631A	10833B
2 meters	10631B	10833C
4 meters	10631C	10833D

Figure 2. Standard HP-IB Cables

Cabling Length Restrictions

In order to ensure proper operation of the bus, two rules must be observed regarding the total length of bus cables when they are connected together:

- The total length of cable permitted with one bus card must be less than or equal to two meters times the number of devices connected together (the interface card is counted as one device).
- The total length of cable must not exceed 20 meters.

For example, there may be up to 4 meters of cable between the first two devices (2 devices × 2 m/device = 4 m). Additional devices may be added using 2-meter cables up to a total of 10 devices (10 device × 2 m/device = 20 meters) using one 4-meter and eight 2-meter cables (4 + (8 × 2) = 20). If more than ten devices are to be connected together, cables shorter than two meters must be used between some of the devices. For example, 15 devices can be connected together using one 4-meter and thirteen 1-meter cables (4 + (13 × 1) = 17). Other combinations may be used as long as both requirements are met.

There are no restrictions to the ways cables may be connected together. However, it is recommended that no more than 3 or 4 piggy-back connectors be stacked together on one device. The resulting structure could exert great force on the connector mounting and cause mechanical damage.

Hardware Conversion Kit

The cable supplied with the 98034 Interface has mounting hardware with metric threads (ISO M3.9x0.6). Earlier bus cables and some HP-IB compatible instruments, however, have cable-mounting hardware with English threads (6-32 UNC). The English hardware is silver while the metric hardware is black. Do not attempt to mate silver and black hardware.

A conversion it is available to replace the mounting hardware on any HP-IB connector with metric threads. Order HP part number 5060-0138.

LOW EMI Cable Adapter

The HP 10834A Adapter helps in applications where limited rear-panel space is available for connecting the new low EMI bus cables. The adapter extends the bus cable about 23 mm away from the rear panel, providing space for other connectors, switches, etc., near the HP-IB connector.

The 10834A Adapter is packaged with some HP instruments, where needed. Contact your HP sales representative for more details.

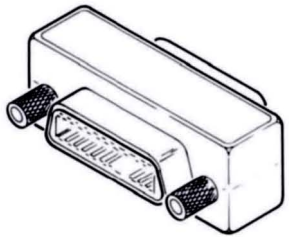


Figure 3. The 10834A Adapter

Select Code

The select code switch is accessible through a small hole on the top of the interface case. The switch is preset to select code 7 at the factory. To change the setting, rotate the switch using a small screwdriver.

> **NOTE**
> The Desktop Computer reserves certain select codes (see the Operating and Programming Manual). Those codes are reserved for internal computer peripherals (display, keyboard, etc). Also do not use the same code for more than one interface.

Interrupt Priority

Some calculator I/O ROMs enable a peripheral-interrupt scheme based on the interface select code. Select codes 2 through 7 have a low-interrupt priority, while select codes 8 through 15 have a high-interrupt priority. If a device on the bus requires fast interrupt service, the interface should be set to a high-priority select code. See the appropriate I/O ROM manual for more details.

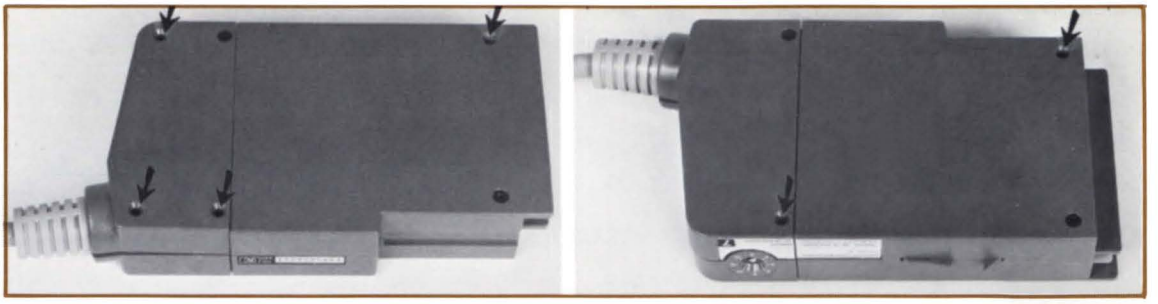
Removing the Interface Covers

Follow these steps to open the interface case:

1. Switch the calculator off; then unplug the interface from both the calculator and the bus.
2. Position the interface as shown in the first photo and remove only the four screws shown. Then flip the interface over and remove only the upper-right and lower-left screws.
3. Carefully seperate the halves of the interface case and position them as shown in the last photo.

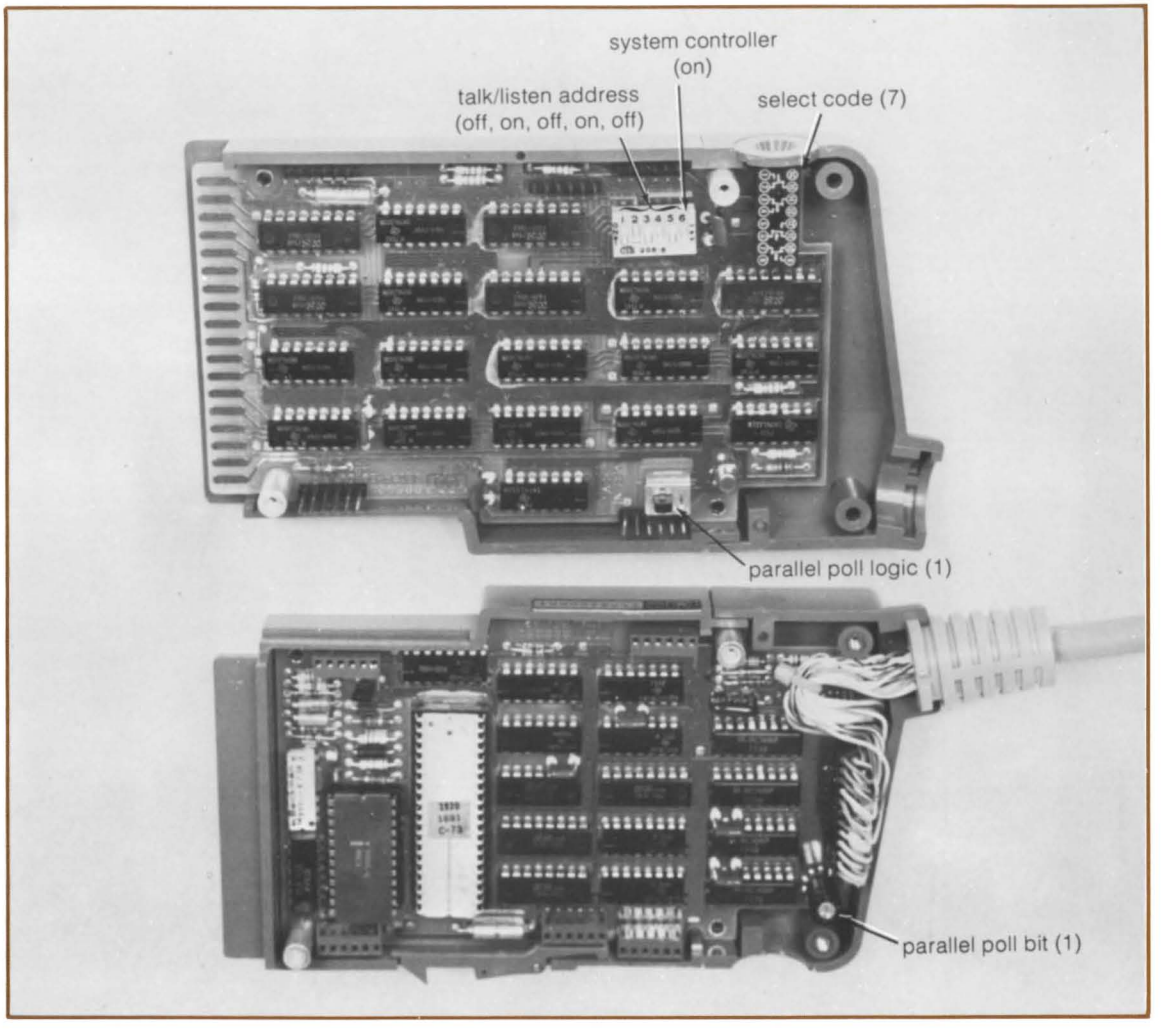
To reassemble the interface:

1. Be sure that all five pin connectors on one board are aligned with their sockets on the other board.
2. Position the cable wires so that they are not crimped as the case halves are pressed together.
3. Secure the cable-end of the case first, using the two long screws. Then replace the other screws.



A. Remove only the four screws shown above.

B. Flip the card over and remove these two screws.



C. Separate the case halves and position them as shown.

Figure 4. Opening the Interface Case (98034A shown)

Changing Talk/Listen Addresses

The bus interface is set to talk address "U" and listen address "5" at the factory. These may be changed to any talk/listen pair of characters listed in the next table by setting switch S3 (1 through 5) on the A1 circuit board. Setting each slide to the "ON" position corresponds to a "0" in the table.

Table 5. Available Bus Addresses and Codes

Address Characters		Address Switch Settings					Address Codes	
Listen	Talk	(5)	(4)	(3)	(2)	(1)	decimal	octal
SP	@	0	0	0	0	0	0	0
!	A	0	0	0	0	1	1	1
"	B	0	0	0	1	0	2	2
#	C	0	0	0	1	1	3	3
$	D	0	0	1	0	0	4	4
%	E	0	0	1	0	1	5	5
&	F	0	0	1	1	0	6	6
'	G	0	0	1	1	1	7	7
(	H	0	1	0	0	0	8	10
)	I	0	1	0	0	1	9	11
*	J	0	1	0	1	0	10	12
+	K	0	1	0	1	1	11	13
,	L	0	1	1	0	0	12	14
−	M	0	1	1	0	1	13	15
.	N	0	1	1	1	0	14	16
/	O	0	1	1	1	1	15	17
0	P	1	0	0	0	0	16	20
1	Q	1	0	0	0	1	17	21
2	R	1	0	0	1	0	18	22
3	S	1	0	0	1	1	19	23
4	T	1	0	1	0	0	20	24
5	U	1	0	1	0	1	21	25 ← preset
6	V	1	0	1	1	0	22	26
7	W	1	0	1	1	1	23	27
8	X	1	1	0	0	0	24	30
9	Y	1	1	0	0	1	25	31
:	Z	1	1	0	1	0	26	32
;	[	1	1	0	1	1	27	33
<	/	1	1	1	0	0	28	34
=	]	1	1	1	0	1	29	35
>	^	1	1	1	1	0	30	36

Enabling System Controller

Switch S3(6) on the A1 circuit board enables the calculator as the system controller. The system controller function is enabled when A1S3(6) is ON. Refer to the preceding photo.

Parallel Poll Switches

Switch S1 on the A2 circuit board determines which data bit is output in response to a parallel poll operation. A2S1 is preset to bit 1 at the factory. To change the setting, rotate the switch using a small screwdriver.

Switch S2 on the A1 circuit board determines the logic level used when sending the parallel poll bit. The switch is preset to use negative-true logic. To use positive-true logic, set A1S2 to the "0" position.

Notes

Chapter 3
Service

Introduction

This chapter contains a description of interface operation and instructions to help you repair the interface. A complete circuit diagram and a list of replaceable parts are at the back of this chapter.

Due to the microprocessor-based organization of this interface, it's recommended that the interface not be repaired to the discrete component level. Instead, run the Functional Test described next, and then the 98034 Test Procedure described in your computer's System Exerciser. If either test indicates a defective interface, use the following Theory of Operation and Circuit Diagram to find the defective assembly.

If you have difficulty repairing the interface or if you would rather have HP repair it, contact the nearest Sales and Service office for assistance; office locations are listed after the circuit diagram.

Functional Test

This test checks operation of most 98034 circuits. To perform a complete test of the interface, follow the 98034 Test Procedure in your computer's System Exerciser.

This test assumes that the interface switches are set to their factory settings:

98034 Factory Settings

Switch	Function	Factory Setting
A1S1	Select Code	7
A1S2	Parallel Poll Sense	Negative-True Logic (position 1)
A1S3 (1 thru 5)	Calculator Address	Talk = U, Listen = 5 (off, on, off, on, off)
A1S3 (6)	System Controller	Enabled (on)
A2S1	Parallel Poll Bit	Bit 1 (least-significant bit)

Refer to Chapter 2 for instructions on setting the switches.

To Test the Interface (9825):

1. Plug the interface card into any I/O slot on the back of the calculator. Verify that either a General I/O ROM or an Extended I/O (with General I/O) ROM is plugged in the calculator.
2. Switch the calculator on and verify the display ⏵ ⊢

   If the ⊢ does not appear, remove the interface and press RESET. If the ⊢ display still does not appear, refer to the 9825 System Test Booklet.
3. When an Extended I/O ROM is plugged in, execute this line and verify the display:

   ```
   rds (7,A,B,C) → D; dsp A,B,C,D
   ```

   0.00 213.00 64.00 76.00

   The first thru fourth status bytes are displayed from left to right, respectively. See page 30 for details on status bytes.

   When only a General I/O ROM is plugged in, execute this line and verify the display:

   ```
   rds (7)
   ```

   76.00
4. If the display does not return after the line is executed, press RESET and rotate the select code switch to 0 and back to 7. Then repeat the appropriate line above.
5. If the display still does not return, or if an incorrect number is returned, the interface card is defective.

> **NOTE**
> The numbers returned in this procedure will be incorrect when the Address and/or System Controller switches are incorrectly set.

To Test the Interface (System 35/45):

1. Plug the interface into any empty I/O slot on the back of the computer. Verify that the I/O ROM is plugged into the computer.
2. Switch the computer on and verify that the cursor appears on the CRT. If the cursor does not appear on the CRT, press CONTROL-STOP. If the cursor still does not appear, refer to your System Exerciser Manual.
3. Execute the following statements:

   ```
   STATUS 7;A,B,C,D
   DISP A,B,C,D
   ```

   the results are

   ```
   0   213   64   76
   ```

   The first thru fourth status bytes are displayed from left to right, respectively. See page 30 for details on status bytes.
4. If the results are not as shown, rotate the select code switch to 0 and back to 7. Repeat step 3.
5. If the results still are not as shown, refer to the System Exerciser Manual for further interface verification procedures.

> **NOTE**
> The numbers returned in this procedure will be incorrect when the Address and/or System Controller switches are incorrectly set.

Replaceable Assemblies

These assemblies are available for direct replacement:

Table 6. Replaceable Assemblies

Assembly	HP Part Number
Calculator I/O Logic Board (A1 or A3)	98034-66503
HP-IB Control Logic Board (A2 or A4)	98034-66504
Cable Assembly:	
98034A	98034-61601
98034B (cable and case-half assembled)	98034-61611

The 98034A was built with 98034-66501 and 98034-66502 boards as A1 and A2 assemblies. The 98034B is built with 98034-66503 and 98034-66504 boards as A3 and A4 assemblies. The 98034A and 98034B are functionally compatible. However, the A1 and A2 assemblies cannot be used in the 98034B. In the 98034A ONLY: The A1 and A3 are interchangeable, and the A2 and A4 are interchangeable.

Calculator I/O Lines

The data and control lines available at the calculator I/O slots are listed on the next page. The lines are also shown in the block diagram on page 22. The bar above each line name indicates that negative-true logic is used.

Table 7. Calculator I/O Lines

Line	Description	Signal Direction (Calc. ⟷ interface)
$\overline{IOD0}$ thru $\overline{IOD7}$	Input/Output Data Lines	⟷
$\overline{PA0}$ thru $\overline{PA3}$	Peripheral Address Lines	→
$\overline{IC1}$ thru $\overline{IC2}$	Register Code Lines	→
$\overline{DOUT}$	Direction of Data Transfer (1 = output)	→
$\overline{IOSB}$	I/O Strobe Line	→
$\overline{FLG}$	Interface Flag (1 = interface ready)	←
$\overline{STS}$	Interface Status (1 = interface present)	←
$\overline{INIT}$	Calculator Initialize (reset)	→
$\overline{IRL}$	Interrupt Request Low (0–7)	←
$\overline{IRH}$	Interrupt Request High (8–15)	←
$\overline{INT}$	Demand Response to Interrupt Poll	→

Bus Lines and Timing

The standard HP-IB signal lines are described next. The function of each line is fully described by IEEE Standard 488-1978.

Data Lines (DIO1–8)

The data lines are used to communicate all data including input, output and program codes, addresses control, and status information between instruments connected to the bus. Data is sent one character (byte) at a time (i.e., byte-serial and bit-parallel) under control of the Transfer Lines. In most instruments, data is based on the 7-bit ASCII code. Unused data lines terminate in a resistor load.

Control Lines (ATN, IFC, SRQ, EOI, and REN)

The five control lines govern the flow of information over the data and transfer lines.

ATN (Attention) is driven by the active controller and indicates whether address commands (ATN is low) or data (ATN is high) are being transmitted.

IFC (Interface Clear) is used only by the system controller to initialize the bus via the Abort message. When IFC is low for at least 100 μs, all talkers and listeners are stopped, the serial poll mode is disabled, and control is returned to the system controller. When IFC is high, it has no effect on the bus operation.

SRQ (Service Request) is driven low by a device to indicate that it wants the attention of the controller. SRQ may be set low at any time except when IFC is low.

EOI (End or Identify) may be used to indicate the end of an instrument's character string. When ATN is high, the addressed talker may indicate the end of its data by setting EOI low at the same time that it places the last byte on the data lines.

REN (Remote Enable) is driven by the system controller and is one of the conditions for operating instruments under remote control. Only instruments capable of remote operation use REN and they monitor it at all times. Instruments that do not use REN terminate the line in a resistor load. The system controller may change the state of REN at any time.

Transfer Lines (NRFD, NDAC, and DAV)

The three transfer (handshake) lines are used to execute the transfer of each byte of information on the data lines. All instruments use these lines and employ an interlocked "handshake" technique to pass information. This allows asynchronous data transfer without timing restrictions being placed on any instrument connected to the bus. Transfer of each byte is accomplished at the speed of the slowest instrument.

NRFD (Not Ready for Data) indicates that all listeners are ready to accept information on the data lines. When NRFD is low, one or more listeners are not ready for data.

NDAC (Not Data Accepted) is high to indicate the acceptance of information on the data lines by all listeners. When NDAC is low, all listeners have not accepted the information.

DAV (Data Valid) indicates the validity of information on the data lines. When DAV is low, the information on the data lines is valid for the listener(s). When DAV is high, the information on the data lines is not valid.

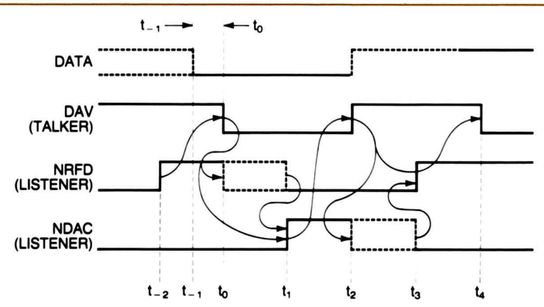
Data Transfer

Transfer of data on the bus is asynchronous. It places no restrictions on the data rates of instruments connected to the bus. The timing and levels required to transfer a byte of information on the data lines are shown in the next figure. Transfer is under the control of three

lines: DAV, NRFD and NDAC. The talker (sender of data) controls the data lines and DAV (Data Valid) and the listeners (acceptors of data) controls both NRFD (Not Ready for Data) and NDAC (Not Data Accepted).

The transfer of a byte of data is initiated by all listeners, signifying they are ready for data, by setting NRFD high. When the talker recognizes NRFD is high and has placed valid data on the data lines, it sets DAV low. When the listener senses that DAV is low and has finished using the data, it sets NDAC high. Notice that the assertive, or action state, of both NRFD and NDAC is high. Since all instruments on the bus have their corresponding lines connected together, all listeners must be in a high state before that line goes high. This wired AND situation allows a talker to recognize when the slowest listener has accepted a byte of data and is ready for the next byte.

The next figure also shows the timing of the transition to the non-assertive state of these lines. A listener may set NRFD low when it recognizes that DAV has been set low; it must do so either before or at the same time it puts NDAC high. The talker may return DAV to its high state after it detects that NDAC is high. A listener may set NDAC low as soon as it recognizes that DAV is high; it must do so either before or at the same time it places NRFD in its high state.



(The curved lines indicate interlocked signal sequence.)

t_{-2} : Listener becomes ready to accept data.

t_{-1} : Talker has put data on the lines.

t_0 : Indicates data is valid.

t_1 : Listener has accepted the data and no longer requires it held valid.

t_2 : Talker indicates the data is no longer valid and may change it.

t_3 : Listener indicates it is ready for new data.

t_4 : A new cycle begins (equivalent to t_0).

t_{-1} to t_0 : Time that data is put on lines before DAV is set low.

Figure 5. HP-IB Three-wire Handshake

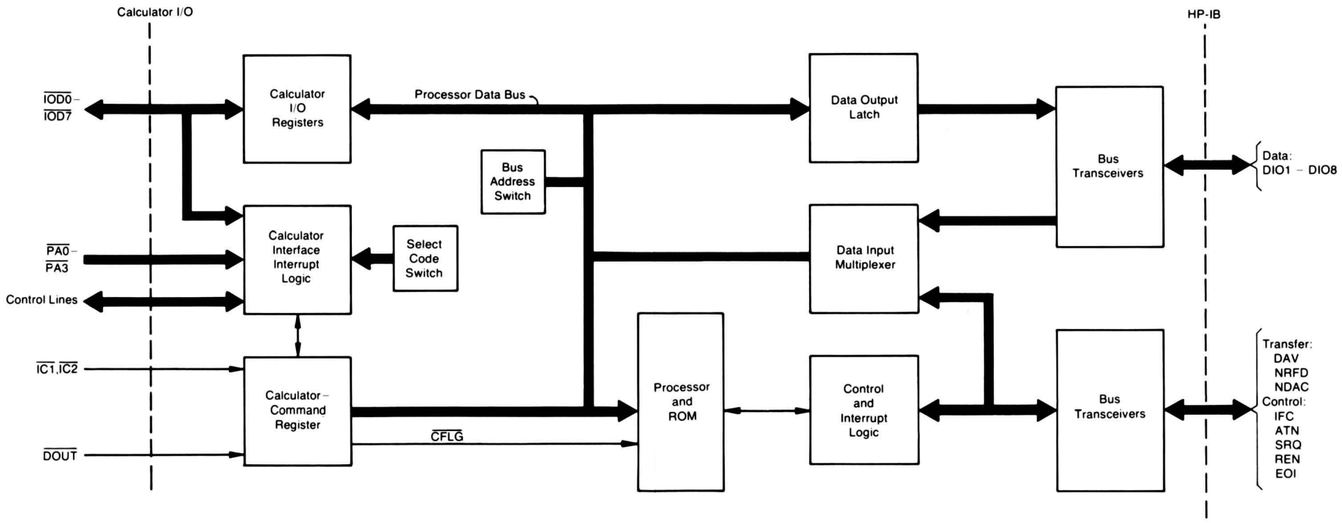


Figure 6. 98034 Simplified Block Diagram

Foldout

Theory of Operation

The 98034 interfaces the calculator to the HP-IB by performing four major functions: interpreting control bytes from the calculator, transferring data bytes from the calculator to the HP-IB, transferring data bytes from the HP-IB to the calculator, and transferring status information to the calculator.

A simplified block diagram of the interface is shown on the left. The diagram shows the interconnections between processor, ROM, I/O registers and other circuits needed to support the processor, calculator I/O and HP-IB.

The processor monitors the status of both the calculator I/O and the HP-IB. It determines if the calculator is requesting an I/O operation by monitoring the CFLG (Calculator Flag) line from the calculator command register. If this signal is true, the processor issues the appropriate instructions to the other modules to decode and execute the requested I/O operation. The processor monitors the status of the HP-IB by periodically sampling its control lines (ATN, SRQ, REN, IFC and EOI) and its transfer lines (DAV, NRFD and NDAC) via the Data Input Multiplexer. If a condition is detected that requires action (for example, a Require Service message) the processor issues the appropriate instructions to complete the operation requested.

Please refer to the Complete Block Diagram on page 33 while reading the remainder of this section.

Select Code Decoder and Switch

The function of the Select Code Decoder is to determine when the interface is addressed by the calculator. The interface responds only when the code on the peripheral address lines, PA$\emptyset$ through PA3, matches the select code set on the select code switch. Receiving the preset code enables the interface to look for an I/O command from the calculator. When the interface is ready for an I/O operation, the interface indicates its presence to the calculator by setting the flag line (FLG) low and setting the status line (STS) low when no error conditions exist on the interface.

I/O Register Decoder and Calculator Command Register

The I/O Register Decoder is a network of gates which interprets the type of I/O operation being requested by the calculator. It determines whether the transfer is an input or output operation by looking at the DOUT line. For an output operation, the data on the calculator input/output data lines (IOD$\emptyset$ through IOD7) is latched into the Calculator Output Data Register when the I/O strobe pulse (IOSB) occurs. For an input operation when the calculator is not conducting an interrupt poll (INT), the data in the Calculator Input Data Register is placed on the calculator data lines. For both input and output, the code on the DOUT, IC1 and IC2 lines is latched into the Calculator Command Register when the I/O strobe pulse (IOSB) occurs.

The Calculator Command Register consists of a 4-bit latch and four open-collector NAND gates. The latch holds the I/O register code (R4 through R7) determined by IC1 and IC2 and the direction of the I/O transfer determined by DOUT. In addition, one bit of the latch is always set when the calculator requests an I/O operation. This bit is buffered through one of the NAND gates and becomes the Calculator Flag line (CFLG). Setting this line true causes the flag line (FLG) to go high, indicating that the interface is busy. The other three NAND gates are used to gate the DOUT, IC1 and IC2 signals onto the processor's data bus when it issues a Read Calculator Command Register (RCCR) instruction. When the processor has executed the requested I/O operation and is ready for another I/O operation, it issues a Clear Calculator Command Register (CCCR) instruction, which clears the Calculator Command Register and readies the interface for another I/O operation.

Calculator I/O Data Registers

The Calculator Output Data Register consists of two 4-bit latches and eight open-collector NAND gates. As described earlier, this register holds the data to be transferred from the calculator to the interface. The data contained in the latches is gated onto the processor data bus when the processor issues a Read Calculator Output Data (RCOD) instruction.

The Calculator Input Data Register consists of two 4-bit latches and eight open-collector NAND gates. The data on the processor data bus is latched into the two 4-bit latches when the processor issues the Send Calculator Input Data (SCID) command. The data in this register is transferred to the calculator input/output data lines when the calculator requests an input operation.

Calculator Interrupt Logic

The Calculator Interrupt Logic allows the interface to request service from the calculator for several conditions which are described later in the section "Controlling the Interface". The Calculator Interrupt Logic is a network of gates and a one-of-eight decoder. This logic pulls the appropriate interrupt request line (IRL or IRH) low when the processor issues a Calculator Interrupt Request (CIRQ) instruction and the calculator is not conducting an interrupt poll (INT). IRL is pulled low when the select code switch is set to an address between 0 and 7, and IRH is pulled low when the switch is set between 8 and 15. When the calculator senses a service request, it conducts an interrupt poll to determine which interface requires service. A poll is conducted when INT is low. When the most-significant bit of the peripheral address (PA3) matches the most-significant address bit from the Select Code switch, the Calculator Interrupt Logic pulls one of the calculator input/output data lines low. The setting of the Select Code switch determines which line is pulled low, as shown in the following table:

Interrupt Request Bits

Select Code	Line Pulled Low
0 or 8	IODØ
1 or 9	IOD1
2 or 10	IOD2
3 or 11	IOD3
4 or 12	IOD4
5 or 13	IOD5
6 or 14	IOD6
7 or 15	IOD7

Control Logic

The Processor, ROM I/O Register Selector, and Oscillator form the control logic portion of this interface. The Processor controls all interface operations by issuing instructions via seven control lines, the 8-bit processor data bus, and selecting I/O registers via the I/O Register Selector. The algorithms for interface control and the implementation of the HP-IB interface functions are contained in the 4096-bit ROM. The Oscillator generates a 2 mHz (approx.) asymmetrical waveform which is used as the main clock for the Processor and as the enable signal for the I/O Register Selector.

The Processor also contains a vectored interrupt structure for conditions that require immediate action. These conditions are described next.

Processor Interrupt Logic

The Processor Interrupt Logic is a network of gates that provides the ability to interrupt the processor for either of two conditions:

- When an Abort message (IFC) is received from the HP-IB or
- When the control line ATN is set true by the controller in charge.

An interrupt occurs for the second condition only when the calculator is not the active controller.

The processor enables the interrupt logic via the Interrupt Enable (IENA) line. When an Abort message is received via the HP-IB, the interrupt causes the processor to generate a 100 μs pulse on the IFC line and then initializes all of the HP-IB interface functions within the interface. The IFC line was previously set true as the result of an I/O operation from the calculator.

When the interface is not the active controller, the processor not only enables the interrupt logic via the Interrupt Enable line, but also sets the Immediate Control line (IMD) true. When an Abort message is received, the interrupt logic generates a vectored interrupt to the algorithm which initializes all of the HP-IB interface functions. In addition, when the controller in charge of the HP-IB sets the ATN line true, the interrupt logic immediately clears the HP-IB Output Data Latch and disables the HP-IB Transceivers for the HP-IB data lines (DIO1 through DIO8), the DAV line, the NRFD line, and the EOI line; then the NDAC line is set low. This leaves the interface ready to receive data from the controller. A vectored interrupt is also generated to the algorithm which controls the acceptance and analysis of the data sent by the controller.

HP-IB Output Data and Control Bus Latches

The HP-IB Output Data Latch consists of two 4-bit latches. Data is transferred from the processor data bus into this 8-bit latch when the processor issues the Send Interface Bus Data (SIBD) command. The outputs of this latch are routed to the HP-IB data lines via the drivers contained in the HP-IB Tranceivers.

The HP-IB Control Bus Latch is a 5-bit latch which holds the bit pattern to be applied to the HP-IB control lines (EOI, ATN, SRQ, REN and IFC). The appropriate bit pattern is transferred from the processor data bus into this latch when the processor issues the Send Interface Bus Control (SIBC) command. This latch consists of one 4-bit latch and one D flip-flop. The outputs of this latch are routed to the bus drivers contained in the HP-IB Transceivers.

HP-IB Address Register

The HP-IB Address Register consists of a hex, tri-state buffer and six switches. Five of the switches are used to set the five least-significant bits of the HP-IB talk/listen address. When each switch is off, its corresponding bit is set to a logical 1. The HP-IB address switches are

connected to the five least-significant bits of the processor data bus (D0 through D4). In addition to the HP-IB address switches, this module also contains the System Controller switch. When this switch is on, the interface assumes the role of system controller. This switch is connected to bit D5 of the processor data bus. The contents of this register is gated onto the processor data bus when the processor issues a Read Interface Bus Address (RIBA) instruction.

Data Input Multiplexer

The function of the Data Input Multiplexer is to route either a data byte (DIO1 through DIO8) or a control byte (EOI, ATN, SRQ, REN, IFC, DAV, NRFD and NDAC) from the HP-IB Transceivers to the processor data bus. The processor selects the data byte by issuing the Read Interface Bus Data (RIBD) command. The control byte is selected when the processor issues the Read Interface Bus Control (RIBC) command.

This module consists of one AND gate and two, quad 2-to-1 multiplexers.

HP-IB Transceivers

The interface uses four bus transceiver modules. Two are used for the HP-IB data lines (DIO1 through DIO8) and two are used for the HP-IB control lines (EOI, ATN, SRQ, REN, IFC, DAV, NRFD and NDOC). These transceivers allow bidirectional flow of data and control information between the interface and the HP-IB. Each transceiver provides four open-collector drivers and four receivers with hysteresis.

Parallel Poll Logic

The Parallel Poll Logic provides the capability to respond to a parallel poll conducted by the controller in charge of the HP-IB. When the controller initiates a parallel poll (ATN and EOI true) and the calculator has requested service from the controller via the SRQ line, the parallel poll logic sends one bit of status to the controller via one data line (DIO1 through DIO8).

This logic consists of a 3-input NAND gate, a slide switch to set the logic level of the bit, and a switch to select which bit on the HP-IB data lines will be used to send the response to the parallel poll.

Initialize Circuit

The Initialize Circuit applies +9 V to the processor after all other power supplies are stable. This condition is indicated by the initialize signal (INIT) from the calculator, and causes the processor to execute an initialize algorithm. If the interface is the system controller, this algorithm issues the Abort message (IFC) and sets the REN line true. If the interface is not the system controller, this algorithm clears all HP-IB interface functions. This circuit also provides a reset pulse to the HP-IB Control Bus Latch.

Controlling the Interface

The calculator controls the interface via four I/O registers, R4 through R7. These registers are memory locations used for the storage of input and output data. It should be noted that these four registers are not dedicated components on the bus interface. Instead, all data passes through the Calculator I/O Registers (see block diagram on page 22) and is temporarily stored in the processor's read/write memory. A store operation from the calculator to any one of these registers transfers the data to the interface previously selected by the peripheral address. A load operation from any of these registers into the calculator transfers the data from the selected interface to the calculator.

The calculator I/O signals IC1 and IC2 determine which I/O register is addressed, as shown below:

IC2	IC1	Register
0	0	R7
0	1	R6
1	0	R5
1	1	R4

The contents of each I/O register are assigned unique roles such as data, status or control (see the next table). These assignments are described in the following pages.

NOTE

The calculator's store and load instructions mentioned here are internal routines, used by I/O ROM to implement the user-language I/O statements and functions. Registers R4 through R7 are not intended to be directly accessible via user-language operations.

Table 8. I/O Register Assignments

Register	Direction	I/O Instruction
R4	IN	Request Data from Bus
	OUT	Send Data to Bus
R5	IN	Interface Status Request
	OUT	Interrupt Byte
R6	IN	Null Operation
	OUT	Send Multiline Interface Message
R7	IN	Get Parallel Poll Byte
	OUT	Send Uniline Interface Message

Send Data

The least-significant eight bits of data contained in the calculator accumulator is transferred to the HP-IB data bus (DIO1 through DIO8) when a Store R4 instruction is executed. Data transfer occurs only if the interface has previously been addressed as a talker on the HP-IB. If the interface has not been addressed to talk, the calculator status line (STS) is cleared.

Receive Data

When a Load R4 instruction is executed, the interface accepts a data byte from the HP-IB and places it in the Calculator Input Data Register. If the interface has not been addressed to listen, however, the calculator status line (STS) is cleared and data is not accepted.

The first Load R4 instruction received by the interface after any other I/O instruction is essentially a request data byte instruction. The data byte placed in the Calculator Input Data Register may be transferred into the least-significant eight bits of the calculator accumulator by executing either a Load R6 instruction or another Load R4 instruction. In this case, both the Load R6 and Load R4 instructions are treated as "no operations" by the interface. The Load R6 causes the interface to remain in the input-data routine, permitting successive Load R4 instructions to rapidly input data. Two Load R4 instructions are needed to input each data byte; the first Load R4 requests the byte and the second Load R4 transfers the byte to the calculator.

Read Interface Status

The calculator can read the status of this interface by executing a sequence of five instructions. The following table shows the sequence of instructions and the information transferred to the calculator:

98034 Read Status Sequence

Instruction	Data Byte
Load R5	HP-IB Interface Signature
Load R6	First Status Byte (Device Clear and Error)
Load R6	Second Status Byte (HP-IB Address)
Load R6	Third Status Byte (HP-IB Control Byte)
Load R6	Fourth Status Byte (Interface Status)

The execution of the Load R5 instruction causes the interface to transfer a data byte to the calculator. The fifth and sixth bits are always set to a logical 1. The remaining six bits are determined by the contents of the Calculator Input Data Register and are ignored. This byte is used to identify the interface. This instruction also causes the interface to enter a read status algorithm, which transfers each of the four additional status bytes to the calculator with successive Load R6 instructions. If the status line (STS) is clear, it will be set by the fourth Load R6 instruction.

The calculator does not have to read all four status bytes. The read status algorithm terminates whenever the interface detects an instruction other than Load R6 before the fourth status byte has been transferred to the calculator. The read interface status instruction must be completed, however, in less than 100 ms. This restriction is necessary to insure that the Abort message (IFC), sent by the controller in charge, is not missed. The bit assignments of the four bytes are summarized on the next page.

First Status Byte:

7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	Device Clear	Ø	Error

Bit 0: Is 1 when error detected.
Bit 2: Is 1 when Device Clear received.

Second Status Byte:

7	6	5	4	3	2	1	0
1	1	0	(MSB)	HP-IB Address			(LSB)

Third Status Byte:

7	6	5	4	3	2	1	0
EOI	REN	SRQ	ATN	IFC	NDAC	NRFD	DAV

Logical 1 indicates corresponding signal line is true.

Fourth Status Byte:

7	6	5	4	3	2	1	0
Service Request	Controller Active	Talker Active	Listener Active	System Controller Set	1	Serial Poll Set	End of Record

Bit 7: Is 1 when the SRQ signal line is true.
Bit 6: Is 1 when the calculator is the active controller.
Bit 5: Is 1 when the calculator is the active talker.
Bit 4: Is 1 when the calculator is an active listener.
Bit 3: Is 1 when the calculator is the active system controller.
Bit 2: Is always 1.
Bit 1: Is 1 when a serial poll is in process.
Bit 0: Is 1 when the EOI (end of record) line is true.

Figure 7. Interface Status Bytes

Interrupt Operation

The 98034 can be enabled to interrupt the calculator by transferring an interrupt-enable byte from the calculator accumulator to the interface with a Store R5 instruction. The bit assignments in the interrupt enable byte are shown in the following table:

7	6	5	4	3	2	1	0
Service Request	Controller Active	Talker Active	Listener Active	Input Register Full	Output Register Empty	Other Interrupt Conditions	Enable EOI

Bit 7: Logical 1 enables interrupt on SRQ.
Bit 6: Logical 1 enables interrupt on active controller.
Bit 5: Logical 1 enables interrupt on active talker.
Bit 4: Logical 1 enables interrupt on active listener.
Bit 3: Logical 1 enables interrupt on input register full.
Bit 2: Logical 1 enables interrupt on output register empty.
Bit 1: Logical 1 enables interrupt when error detected, device clear or selective device clear/received (when not active controller), or EOI received.
Bit 0: Enable EOI to clear status line (STS).

Figure 8. Interrupt Enable Byte

When the interface receives a Store R5 instruction, the interrupt enable byte is transferred from the Calculator Output Data Register to an internal read/write register in the processor. The interrupt enable algorithm then checks the byte against existing conditions to determine if an immediate interrupt should be generated. Any of the following conditions cause an immediate interrupt:

- SRQ (service request) detected.
- Interface is active controller.
- Interface is active talker.
- Interface is active listener.
- Output register empty.

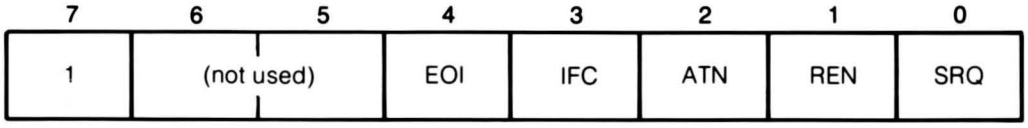
The calculator status line (STS) is cleared when the interface generates an interrupt for any of the above five conditions. The status line is only cleared on the first output-register-empty interrupt. All subsequent output-register-empty interrupts will have status set.

The interrupt request from the interface (IRL or IRH) can only be cleared by executing a Load R6 instruction. If the status line has been cleared as the result of an interrupt, it can be set by reading the interface status.

Sending Interface Messages

When a Store R6 instruction is executed, the eight least-significant bits of the data contained in the calculator are transferred to the Calculator Output Data Register on the interface. The interface interprets this instruction as a command to send a multiline interface message to other devices on the HP-IB. If the interface is the active controller, the ATN line on the HP-IB is then set true and the byte in the Calculator Output Data Register is transferred to the HP-IB. After this multiline message has been transferred, the ATN line remains true until either an instruction other than Store R6 is received by the interface or a Pass Control message (TCT) is transferred to another device on the HP-IB with a Store R6 instruction. When the calculator is not the active controller when the Store R6 instruction is received, the interface clears the status line (STS) to indicate an error.

The interface sends uniline interface messages to other devices on the HP-IB when the calculator executes a Store R7 instruction. If the byte received via a Store R7 instruction has the eighth bit set to a logical 1, the remaining bits in the byte are sent as uniline messages, as shown in the following diagram:



Request Service

When the eighth bit of the byte received with a Store R7 instruction is set to a logical 0, the instruction is interpreted as a Require Service message. The seven least-significant bits of this byte are stored in one of the processor's read/write registers. This byte is transferred to the controller in charge when a serial poll is conducted. If the seventh bit of the byte is a logical 1, the interface automatically sets the SRQ line true and requests service from the controller in charge.

Parallel Poll

The calculator can conduct a parallel poll when it is the controller in charge. A parallel poll is initiated by setting both the ATN and EOI lines true. The calculator can accomplish this by executing a Store R7 instruction with the appropriate byte, as described in the Send Interface Messages section. Once a parallel poll has been initiated, the Status Bit message on the HP-IB must be transferred to the Calculator Input Data Register. This occurs when the calculator executes a Load R7 instruction. The byte that represents the parallel poll response is then transferred to the calculator with a Load R6. The parallel poll is terminated when the calculator executes a Store R7 instruction with the appropriate byte to clear the ATN and EOI lines.

Notes

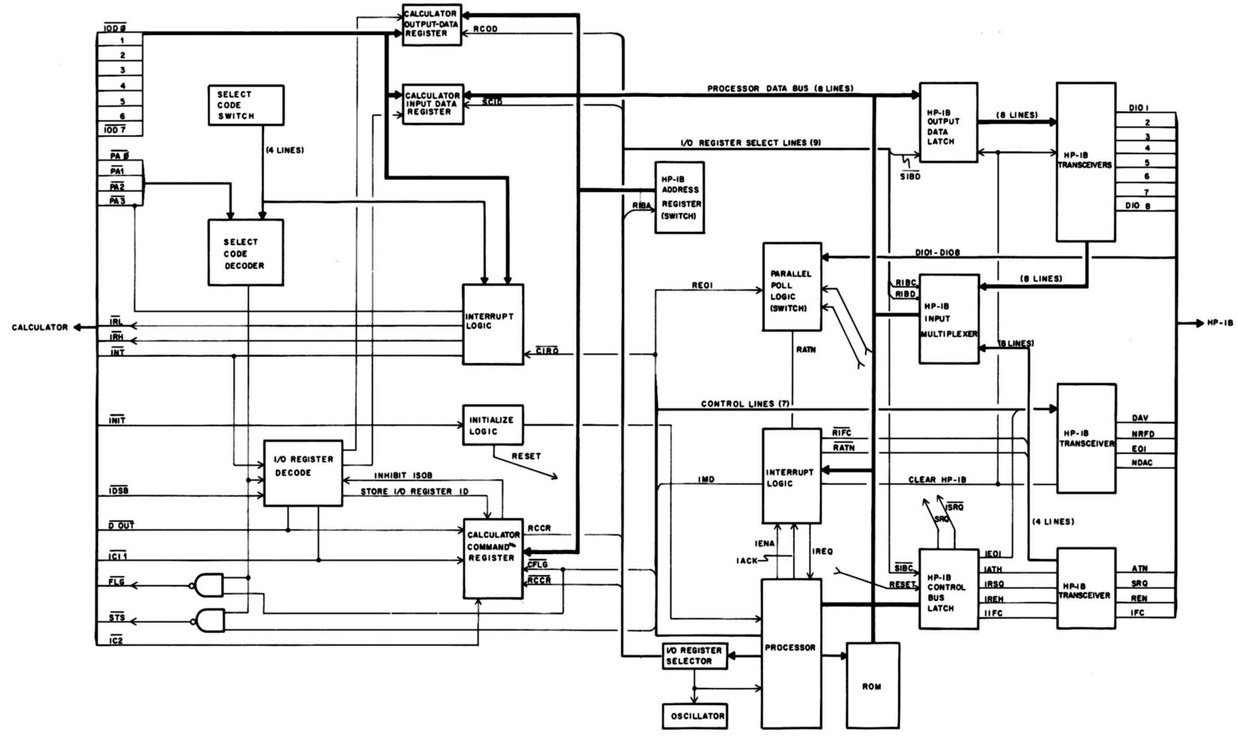


Figure 9. 98034 Detailed Block Diagram

98034A Interface Assemblies

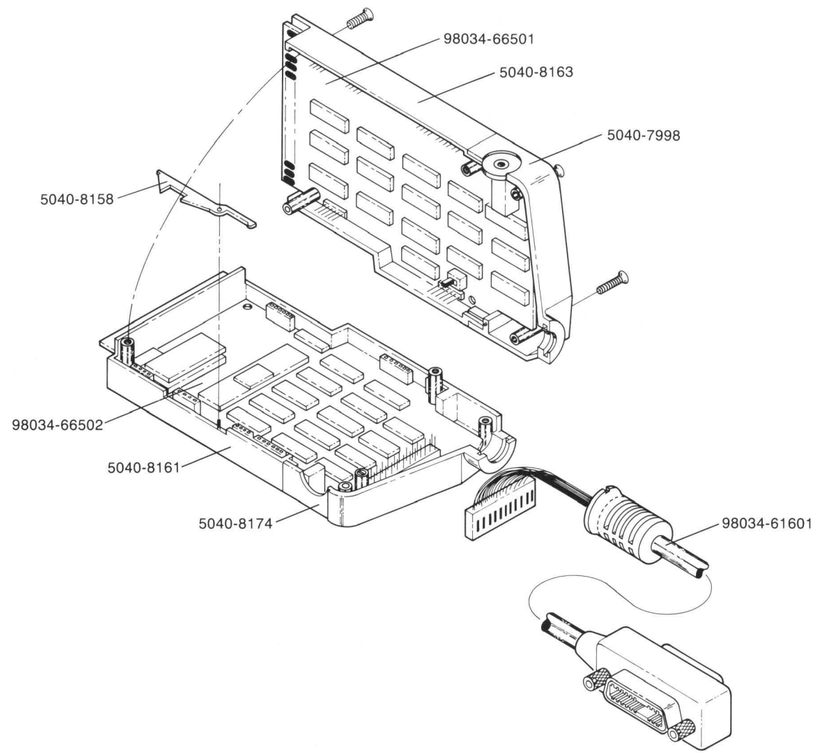


Table 9a. 98034A Replaceable Parts

-hp- PART NO.	TQ	DESCRIPTION
98034-61601	**1**	**Cable Assembly**
5040-8161	1	Cover, Plastic: Left Front Housing
5040-8163	1	Cover, Plastic: Right Front Housing
5040-8174	1	Cover, Plastic: Left Rear Housing
5040-7998	1	Cover, Plastic: Right Rear Housing
2200-0510	2	Screw: 4-40, .75 inches long, Flat-head
2200-0536	8	Screw: 4-40, .44 inches long, Flat-head
5040-8158	1	Latch, Plastic
7120-5800	1	Label, Front Housing
7120-5799	1	Label, Rear Housing

98034B Interface Assemblies

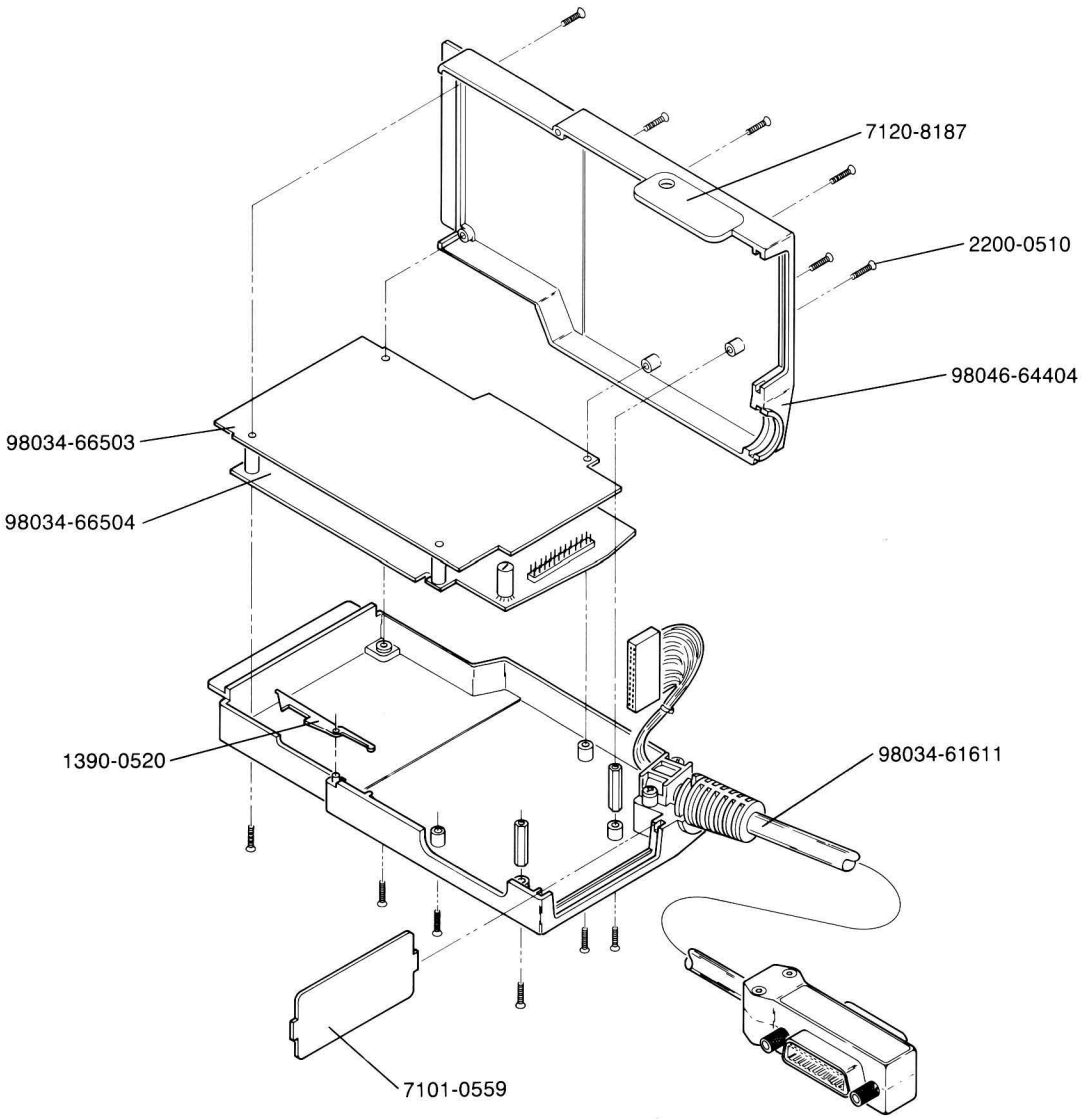
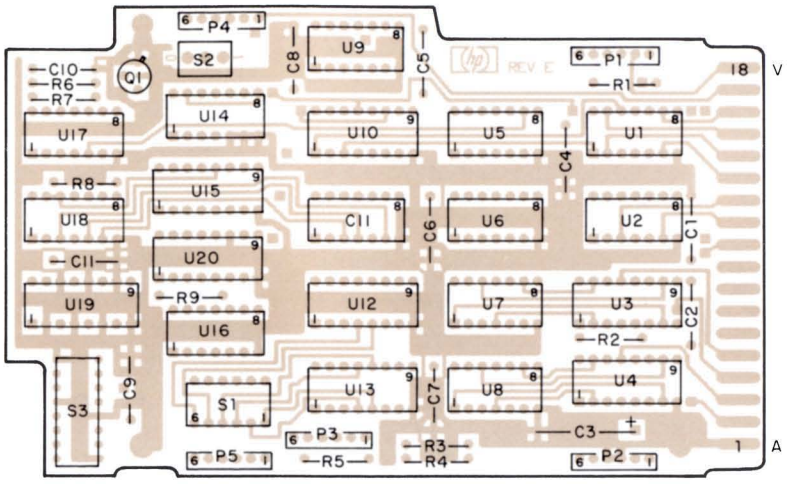


Table 9b. 98034B Replaceable Parts

-hp- PART NO.	TQ	DESCRIPTION
98034-61611	1	Cable Assembly with Left Half-Case
98046-64404	1	Right Half-Case
98034-66503	1	I/O Logic PC Assembly
98034-66504	1	HP-IB Control PC Assembly
1390-0520	1	Spring Latch
7101-0559	1	Rear Plate
7120-5911	1	Warning Label
7120-8187	1	98034B Label
2200-0510	10	Screw, 4-40, .75-Inch Long

Notes



COMPONENT SIDE
A1/A3

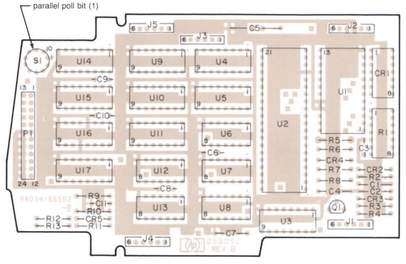
HP Part No. 98034-66501 Rev E (98034A)
HP Part No. 98034-66503 Rev B (98034B)

Table 9c. A1/A3 Replaceable Parts

REFERENCE DESIGNATOR	-hp- PART NO.	CHECK DIGIT	TQ	DESCRIPTION
A1	**98034-66501**	**5**	**1**	**PC Assembly, Computer I/O Logic**
A3	98034-66503	6	1	PC Assembly, Computer I/O Logic (98034B)
A1C1,C2	0160-3847	0	2	Cap, Fixed: 0.01μF, 100V
A1C3	0180-0106	9	1	Cap, Fixed: 60μF, 6V
A1C4-C11	0160-4571	8	8	Cap, Fixed: 0.1μF, 100V
A1P1	1251-4257	1	5	Plug: 6 pin
A1Q1	1854-0019	3	1	Transistor: NPN, Si
A1R1	0683-5625	3	1	Res, Fixed: 5.6KΩ, 5%, ¼W
A1R2-R5,R8	0683-2225	8	5	Res, Fixed: 2.2KΩ, 5%, ¼W
A1R6	0683-1025	9	1	Res, Fixed: 1KΩ, 5% ¼W
A1R7	0683-4725	2	1	Res, Fixed: 4.7KΩ, 5% ¼W
A1R9	0683-3325	6	1	Res, Fixed: 3.3KΩ, 5%, ¼W
A1SW1	3101-2097	8	1	Switch, 6PST DIP: Address & System Controller
A1SW2	3101-1341	3	1	Switch, 1PDT: Parallel Poll Sense
A1SW3	3101-3364	4	1	Switch, 4PDT: Select Code
A1U1	1820-1297	0	1	IC: 74LS266, Quad NOR Gate
A1U2,U6-U8, U11,U16,U18 A1U3,U4	1820-1198	0	7	IC: SN74LS03N, Quad NAND Gate
U12,U13	1820-1562	2	4	IC: MM74C175N, 4-bit Register
A1U5	1820-1199	1	1	IC: 74LS04A, Hex Inverter
A1U9	1820-1284	5	1	IC: SN74LS55, And-or-Invert Gates
A1U10	1820-1427	8	1	IC: SN74LS56, Decoder
A1U14	1820-1144	6	1	IC: SN74LS02N, Quad NOR Gate
A1U15	1820-1195	7	1	IC: 74S175, 4-bit Register
A1U17	1820-1203	8	1	IC: SN74LS11N, 3-input AND Gate
A1U19	1820-1266	3	1	IC: MM80C97N, Hex Buffer
A1U20	1820-1437	0	1	IC: SN74LS221, Dual One Shot

Table 9d. A2/A4 Replaceable Parts

REFERENCE DESIGNATOR	-hp- PART NO.	CHECK DIGIT	TQ	DESCRIPTION
A2	**98034-66502**	**6**	**1**	**PC Assembly: HP-IB Control Logic**
A4	98034-66504	5	1	PC Assembly: HP-IB Control Logic (98034B)
A2C1,C2	0180-0210	6	2	Cap, Fixed: 3.3μF, 15V
A2C3,6,8-10, C12-C14,C16	0160-4571	8	9	Cap, Fixed: 0.1μF, 100V
A2C4,C17	0160-3334	9	2	Cap, Fixed: 0.01μF, 50V
A2C5	0180-0106	9	1	Cap, Fixed: 60μF, 6V
A2C7	0160-3847	9	1	Cap, Fixed: 0.01μf, 25V
A2C11	0160-0495	7	1	Cap, Fixed: 390pF, 300V, ±1%
A2C15	0121-0180	5	1	Cap, Variable: 15 to 60pF
A2CR2,CR3, CR5	1901-0040	1	3	Diode: Si, 0.05A, 30V
A2CR4	1902-3158	0	1	Diode, Zener: 9.76V, ±2% @ 10ma
A2P1-P5	1251-4215	1	5	Connector: 6-pin
A2J1	1251-4333	4	1	Connector: 24-pin
A2Q1	1853-0016	8	1	Transistor: PNP, Si
A2Q2	1854-0071	7	1	Transistor: PNP, Si
A2R2	0683-5615	1	1	Res, Fixed: 560Ω, 5%, ¼W
A2R3	0683-3325	6	1	Res, Fixed: 3.3KΩ, 5% ¼W
A2R4,R9,R12	0683-2225	3	3	Res, Fixed: 2.2KΩ, 5%, ¼W
A2R5	*		1	(Optimum Value Selected at the factory)
A2R6	0683-1815	5	1	Res, Fixed: 1.8KΩ, 5%,¼W
A2R7	0683-2025	1	1	Res, Fixed: 2.0KΩ, 5%, ¼W
A2R8	0683-5625	3	1	Res, Fixed: 5.6KΩ, 5%, ¼W
A2R10	0698-3225	6	1	Res, Fixed: 1.43KΩ, 1%, ⅛W
A2R11	0698-3557	7	1	Res, Fixed: 806Ω, 1%, ⅛W
A2R13	0683-1035	1	1	Res, Fixed: 10KΩ, 5%, ¼W
A2R14	0683-1515	3	1	Res, Fixed: 150Ω, 5%, ⅛W
A2R15	0693-1515	3	1	Res, Fixed: 150Ω, 5%, ¼W
A2SW1	3100-3378	8	1	Switch, 1P10T: Parallel Poll Bit
A2U1	1816-1242	6	1	IC: PROM
A2U2	1820-1692	9	1	IC: Nanoprocessor
fetch A2U3	1820-1216	3	1	IC: SN74LS138N, Decoder
A2U4,U5	1820-1562	2	2	IC: MM74C175N, 4-bit Register
A2U6	1820-1112	8	1	IC: SN74LS74, Dual Flip-flop
A2U7	1820-1201	6	1	IC: SN74LS08N, Quad And Gate
A2U8	1820-1199	1	1	IC: 74LS04N, Hex Inverter
A2U9,U10	1820-1439	2	2	IC: SN74LS258N, Quad Data Selector
A2U11	1820-1192	4	1	IC: SN74LS175, Quad D Flip-flop
A2U12	1820-1417	6	1	IC: 74LS26N, Quad HV NAND Gate
A2U13	1820-1425	6	1	IC: SN74LS132N, Quad NAND Schmitt
A2U14,U17	1820-1689	4	1	IC: MC3446P, HP-IB Bus Buffer
A2U18	1810-0326	3	1	Resistor/Diode Network



COMPONENT SIDE A2

HP Part No. 98034-66502 Rev B

When replacing the nanoprocessor chip (P/N 1820-1692) be sure to provide the correct value for A2R5. This resistor determines the amount of back-bias voltage that the nanoprocessor receives. The correct value for back-bias voltage is printed on the nanoprocessor chip and will vary from approximately −2.0 volts to −5.0 volts. The following table provides the part numbers and resistor values to be used to provide the correct voltage.

Table 9e. Replacement Values for A2R5

BACK-BIAS VOLTAGE	RESISTOR VALUE	A2R5 PART NUMBER	CHECK DIGIT
−2.0V	365Ω	0757-0412	3
−2.5V	475Ω	0757-0415	6
−3.0V	604Ω	0757-0161	9
−3.5V	750Ω	0757-0420	3
−4.0V	909Ω	0757-0422	5
−4.5V	1100Ω	0757-0424	7
−5.0V	1300Ω	0757-0426	9

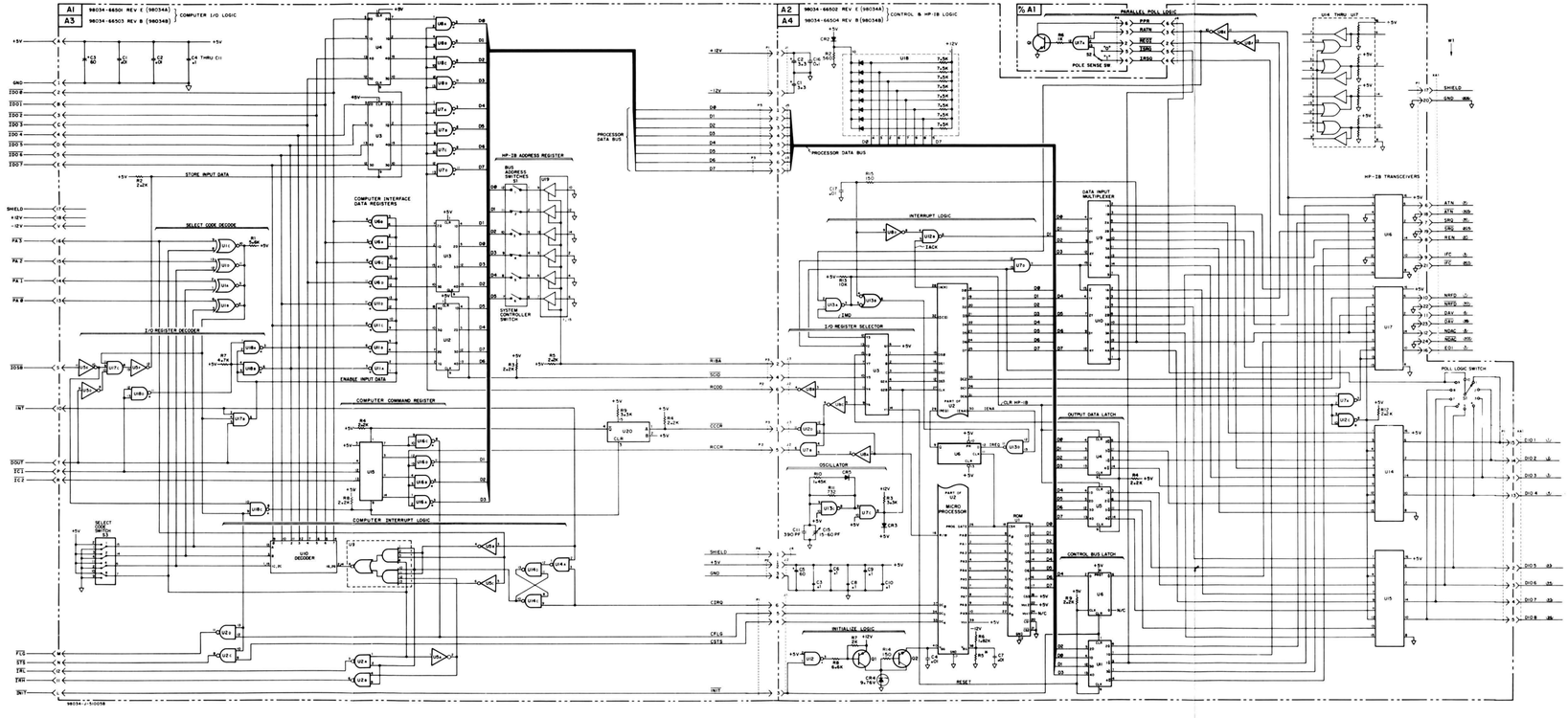
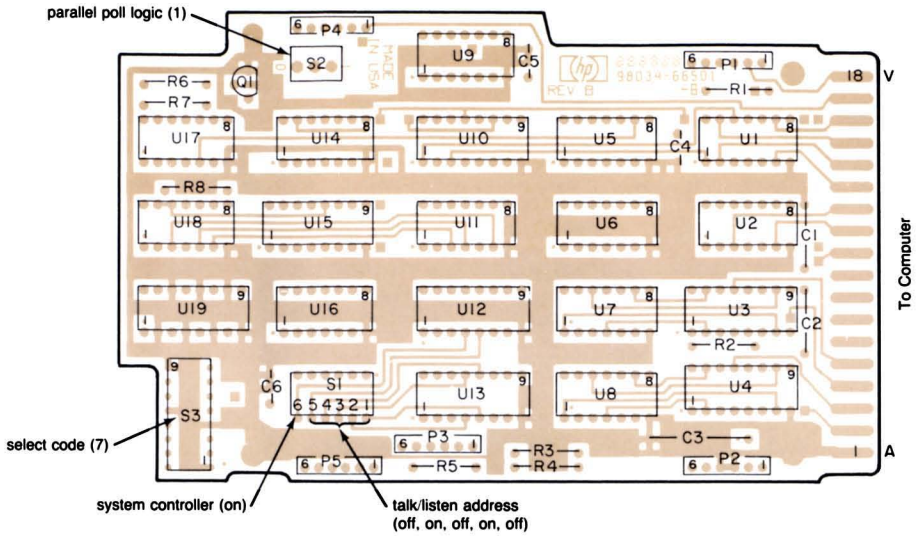


Figure 10. 98034 Circuit Diagram

Notes

Table 10. 98034A Rev. B Replaceable Parts

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A1	98034-66501	1	PC Assembly, Calculator I/O Logic.
A1C1,C2	0160-3847	2	Cap, Fixed: 0.01μF, 100V.
A1C3	0180-0106	1	Cap, Fixed: 60μF, 6V.
A1C4,C5,C6	0160-3622	3	Cap, Fixed: 0.1μF, 100V.
A1P1-P5	1251-4257	5	Plug: 6 pin.
A1Q1	1854-0019	1	Transistor: NPN, Si.
A1R1	0683-5625	1	Res, Fixed: 5.6KΩ, 5%, 1/4W.
A1R2-R5,R8	0683-2225	5	Res, Fixed: 2,2KΩ, 5%, 1/4W.
A1R6	0683-1025	1	Res, Fixed: 1KΩ, 5%, 1/4W.
A1 R7	0683-4725	1	Res, Fixed: 4.7KΩ, 5%, 1/4W.
A1SW1	3101-2097	1	Switch, 4PDT: Select Code.
A1SW2	3101-1341	1	Switch, 1PDT: Parallel Poll Sense.
A1SW3	3100-3364	1	Switch, 6 Gang: Address & System Controller.
A1U1	1820-1297	1	IC: 74LS266, Quad NOR Gate.
A1U2,U6-U8, U11,U16,U18	1820-1198	7	IC: SN74LS03N, Quad NAND Gate.
A1U3,U4, U12,U13	1820-1562	4	IC: MM74C175N, 4-bit Register.
A1U5	1820-1199	1	IC: 74LS04A, Hex Inverter.
A1U9	1820-1284	1	IC: SN74LS55.
A1U10	1820-1427	1	IC: SN74LS56, Decoder.
A1U14	1820-1144	1	IC: SN74LS02N, Quad NOR Gate.
A1U15	1820-1195	1	IC: 74S175, 4-bit Register.
A1U17	1820-1203	1	IC: SN74LS11N, 3-input AND Gate.
A1U19	1820-1266	1	IC: MM80C97N.
A2	98034-66502	1	PC Assembly: HP-IB Control Logic.
	98034-69502		PC Assembly without U1 and U2.
A2C1,C2	0180-0210	2	Cap, Fixed: 3.3μF, 15V.
A2C3,C6, C8-C10	0160-3622	5	Cap, Fixed: 0.1μF, 100V.
A2C4	0160-3334	1	Cap, Fixed: 0.01μF, 50V.
A2C5	0180-0106	1	Cap, Fixed: 60μF, 6V.
A2C7	0160-3847	1	Cap. Fixed: 0.01μF, 25V.
A2C11	0160-3482	1	Cap, Fixed: 430 PF, 300V, 1%.
A2CR1	1906-0075	1	Diode Array.
A2CR2,CR3, CR5	1901-0040	3	Diode: Si, 0.05A, 30V.
A2CR4	1902-3018	1	Diode: Zener.
A2P1-P5	1251-4215	5	Connector: 6 pin.
A2J1	1251-4333	1	Connector: 24 pin.
A2Q1	1853-0016	1	Transistor: PNP, Si.
A2R1	1810-0264	1	Resistor Network.
A2R2	0683-5615	1	Res, Fixed: 560Ω, 5%, 1/4W.
A2R3	0683-3325	1	Res, Fixed: 3.3KΩ, 5%, 1/4W.
A2R4,R9,R12	0683-2225	3	Res, Fixed: 2.2KΩ, 5%, 1/4W.
A2R5	*	1	(Optimum value selected at the factory. See page 39.)
A2R6	0683-1815	1	Res, Fixed: 1.8KΩ, 5%, 1/4W.
A2R7	0683-2025	1	Res, Fixed: 2KΩ, 5%, 1/4W.
A2R8	0683-5625	1	Res, Fixed: 5.6KΩ, 5%, 1/4W.
A2R10	0698-3225	1	Res, Fixed: 1430Ω, 1%, 1/8W.
A2R11	0698-3557	1	Res, Fixed: 806Ω, 1%, 1/8W.
A2R13	0683-1035	1	Res, Fixed: 10KΩ, 5%, 1/4W.
A2SW1	3100-3378	1	Switch, 1P10T: Parallel Poll Bit.
A2U1	1816-0868	1	IC: PROM.
A2U2	1820-1691	1	IC: Nanoprocessor.
A2U3	1820-1216	1	IC: SN74LS138N
A2U4,U5,U11	1820-1562	3	IC: MM74C175N, 4-bit Register.
A2U6	1820-1753	1	IC: MM74C74N
A2U7	1820-1201	1	IC: SN74LS08N
A2U8	1820-1199	1	IC: 74LS04N, Hex Inverter.
A2U9,U10	1820-1439	2	IC: SN74LS258N
A2U12	1820-1417	1	IC: 74LS26N
A2U13	1820-1425	1	IC: SN74LS132N
A2U14-U17	1820-1689	1	IC: MC3446P



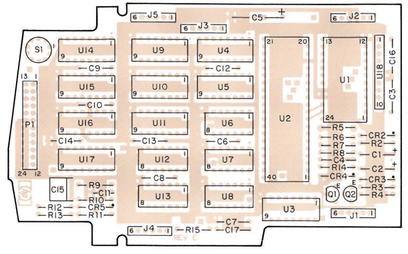
COMPONENT SIDE

A1

HP Part No. 98034-66501 Rev B

NOTE

98034-66501 Rev. B and Rev. C boards are electrically identical. To convert a Rev. A board to Rev. B/C, lift pin 5 on U14 and connect a jumper from U14 pin 5 to U14 pin 7.



COMPONENT SIDE
A2

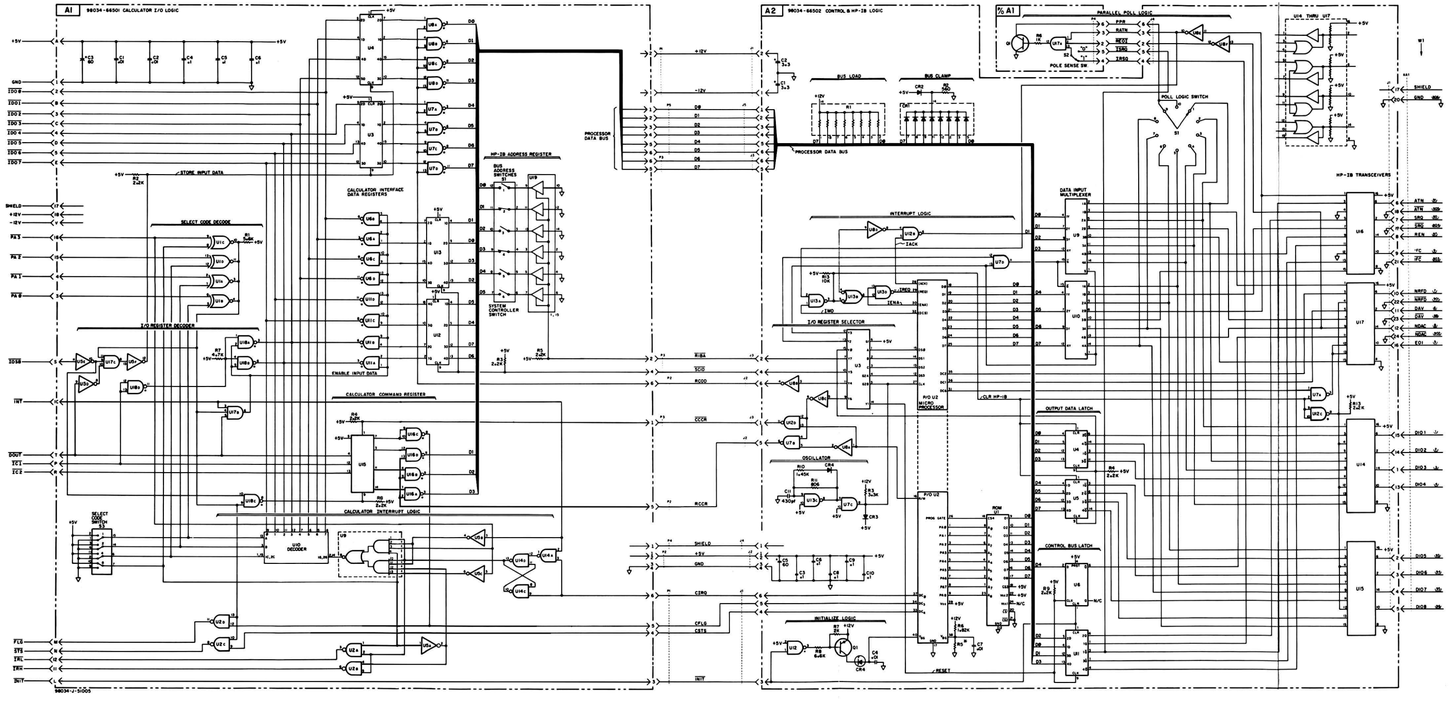
HP Part No. 98034-66502 Rev E (98034A)
HP Part No. 98034-66504 Rev B (98034B)

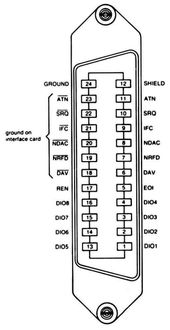
Schematic Notes:

1. Unless indicated otherwise, resistor values are shown in ohms and capacitor values are shown in microfarads.
2. See Chapter 2 before changing the setting of switches.
3. Wire color code is the same as resistor color code: The first number indicates the base color, second number indicates the wider strip, and third color indicates the narrower strip (e.g., 924 = white, red, yellow).

0 = Black	2 = Red	4 = Yellow	6 = Blue	8 = Grey
1 = Brown	3 = Orange	5 = Green	7 = Violet	9 = White

4. A2R5 is selected to maintain the processor's V_{BG} voltage in the range of −2 thru −5 volts. Typical values for A2R5 are from 365Ω (−2V) thru 1.3KΩ (−5V).





HP-IB Cable Pinouts

Figure 11. 98034A Circuit Diagram (Rev B)

98034 HP-IB Interface

Installation and Service Manual

HEWLETT PACKARD

Part No. 98034-90001
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